

**Amendments to the Specification:**

Please replace the paragraph beginning at page 5, line 9 with the following paragraph:

Fig. 1 is a schematic illustration of a conventional power-gating technique employed in a write data driver power-gating circuit in which large P-channel and N-channel power-gating transistors are used to couple and decouple the write data driver to respective VCC and VSS sources in Active and Sleep Modes of operation; [[and]]

Please replace the paragraph beginning at page 5, line 16 with the following paragraph:

Fig. 2 is a schematic illustration of an exemplary implementation of the high speed power-gating technique of the present invention for use, for example, in a comparable write data driver circuit in which the output stage is coupled directly to VCC and VSS and the gate of the output stage N-channel device is driven below VSS in Sleep Mode[. ]; and

Please add the following new paragraph after line 22 on page 5:

Fig. 3 is a schematic illustration of an output stage for a write data driver circuit in which the output stage is coupled directly to VCC and VSS and the gate of the output stage N-channel device is driven above VCC in a Sleep Mode.

Please replace the paragraph beginning at page 10, line 14, with the following amended paragraph:

Although, in the representative embodiment shown, the gate of the N-channel transistor of the output stage 224 is shown as being driven below VSS, the principles of the present invention would likewise pertain to those circuit implementations (FIG. 3) wherein the gate of the output P-channel transistor of the output stage 224 were also, or alternatively, driven above VCC (e.g.  $VCC + 0.3V$ ).